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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/764,243	01/19/2001	Michael C. Stephens JR.	VISA-48	6973

28112 7590 10/28/2003

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/764,243	STEPHENS ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- Th MAILING DATE of this communication appears on th cover sheet with the corresp ndenc addr ss --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 14, 2003 has been entered.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-24 are rejected under 35 U.S.C. 102(b) as being anticipated by Dasse et al., U.S. Patent 5,654,588.

1. Pertaining to claim 1, Dasse discloses a semiconductor method as claimed. See **FIGS. 1-16**, where Dasse teaches a method of detecting a reticle option layer in an integrated circuit device comprising: measuring the current through a first MOS transistor in an integrated circuit device by forcing a test voltage on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first MOS transistor is not parametrically affected by a reticle option layer; measuring the current through a second MOS transistor in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected together, wherein the source of

said second MOS transistor is connected to a reference voltage, and wherein said second MOS transistor is parametrically affected by said reticle option layer; and

comparing said current through said first MOS transistor and said current through said second MOS transistor to detect the presence of said reticle option layer in said integrated circuit device (column 23, lines 27-30).

Pertaining to claim 2, Dasse teaches the method according to Claim 1 wherein said reticle option layer comprises a threshold voltage implantation (column 8, lines 36-47). Please note that it is well known in the art that ROM cells are programmed by implanting a threshold voltage to program the memory cell.

2. Pertaining to claim 3, Dasse teaches the method according to Claim 1 wherein said reticle option layer comprises one of the group of: polysilicon, metal, and threshold implantation.

3. Pertaining to claim 4, Dasse teaches the method according to Claim 1 wherein said first MOS transistor and said second MOS transistor are the same size, the same direction and in close proximity.

4. Pertaining to claim 5, Dasse teaches the method according to Claim 1 wherein said reticle option layer comprises a combination of reticle layers.

5. Pertaining to claim 6, Dasse teaches the method according to Claim 5 wherein said combination of reticle layers comprises the group of: polysilicon, metal, and threshold implantation.

6. Pertaining to claim 7, Dasse teaches the method according to Claim 1 wherein said measuring of said current through said first MOS transistor and said measuring of said current

through said second MOS transistor is by directly probing the die of said integrated circuit device.

7. Pertaining to claim 8, Dasse teaches the method according to Claim 1 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by probing an output pin of packaged said integrated circuit device.

8. Pertaining to claim 9, Dasse teaches the method according to Claim 1 wherein said first MOS transistor and said second MOS transistor comprise one of the group of: NMOS transistors and PMOS transistors.

9. Pertaining to claim10, Dasse discloses a semiconductor device substantially as claimed. Dasse teaches a method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

measuring the current through a first MOS transistor
in an integrated circuit device by forcing a test voltage on the drain and the gate wherein said gate and said drain of said first MOS transistor are connected together, wherein the source of said first MOS transistor is connected to a reference voltage, and wherein said first
MOS transistor has the a first threshold voltage implantation but not the threshold voltage implantation reticle option layer; measuring the current through a second MOS transistor
in said integrated circuit device by forcing same said test voltage on the drain and the gate wherein said gate and said drain of said second MOS transistor are connected together, wherein the source of said second MOS transistor is connected to a reference voltage, and wherein said

second MOS transistor has both a threshold voltage implantation and said threshold voltage implantation reticle option layer; and comparing said current through said first MOS transistor and said current through said second MOS transistor to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device (column 23, lines 27-30).

10. Pertaining to claim 11, Dasse teaches the method according to Claim 10 wherein said first MOS transistor and said second MOS transistor are the same size, the same direction and in close proximity.

11. Pertaining to claim12, Dasse teaches the method according to Claim 10 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by directly probing the die of said integrated circuit device.

12. Pertaining to claim13, Dasse teaches the method according to Claim 10 wherein said measuring of said current through said first MOS transistor and said measuring of said current through said second MOS transistor is by probing an output pin of packaged said integrated circuit device.

13. Pertaining to claim 14, Dasse teaches the method according to Claim 10 wherein said first MOS transistor and said second MOS transistor comprise one of the group of: NMOS transistors and PMOS transistors.

14. Pertaining to claim15, Dasse discloses a semiconductor process substantially as claimed. Dasse teaches a method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first NMOS transistor in an integrated

circuit device in a first test mode so that the voltage at the drain and the gate of said first NMOS transistor may be measured at an output pin of said integrated circuit device wherein said gate and said drain of said first NMOS transistor are connected together, wherein the source of said first NMOS transistor is connected to ground, and wherein said first NMOS transistor has the a first threshold voltage implantation but not the threshold voltage implantation reticle option layer; measuring said voltage at said output pin in said first test mode when an internal a first voltage is connected to said drain and said gate through a first internal a first resistance; selecting a second NMOS transistor in said integrated circuit device in a second test mode so that the voltage at the drain and the gate of said second NMOS transistor may be measured at said output pin of said integrated circuit device wherein said gate and said drain of said second NMOS transistor are connected together, wherein the source of said NMOS transistor is connected to ground, and wherein said second NMOS transistor has both said a first

threshold voltage implantation and said threshold voltage implantation reticle option layer; measuring said voltage at said output pin in said second test mode when said internal a first voltage is connected to said drain and said gate through a second internal a first resistance; and comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device (column 23, lines 27-30).

15. Pertaining to claim16, Dasse teaches the method according to Claim 15 wherein said selecting of said first NMOS transistor is by a multiplex circuit and wherein said selecting of said second MMOS is by a multiplex circuit.

16. Pertaining to claim17, Dasse teaches the method according to Claim 15 further comprising:

amplifying said voltage at said drain and said gate of said first NMOS transistor and said second NMOS transistor to thereby generate an amplified drain and gate voltage at said output pin.

17. Pertaining to claim18, Dasse the method according to Claim 15 wherein said first NMOS transistor and said second NMOS transistor are the same size, the same layout orientation, and in close proximity.

18. Pertaining to claim19, Dasse teaches the method according to Claim 15 wherein said first internal resistance and said second internal resistance comprise the same resistance value.

19. Pertaining to claim 20, Dasse teaches a semiconductor process substantially as claimed. Dasse teaches a method of detecting a threshold voltage implantation reticle option layer in an integrated circuit device comprising:

selecting a first PMOS transistor in an integrated circuit device in a first test mode so that the voltage at the drain and the gate of said first PMOS transistor may be measured at an output pin of said integrated circuit device wherein said gate and said drain of said first NMOS transistor are connected together, wherein the source of said first PMOS transistor is connected to an internal a first voltage, and wherein said first PMOS transistor has the a first threshold voltage implantation but not the threshold voltage implantation reticle option layer;

measuring said voltage at said output pin in said first test mode when said drain and said gate are connected to ground through a first internal a first resistance; selecting a second PMOS transistor in said integrated circuit device in a second test mode so that the voltage at
the drain and the gate of said second PMOS transistor may be measured at said output pin of said integrated circuit device wherein said gate and said drain of said second PMOS transistor are connected together, wherein the source of said PMOS transistor is connected to said internal a first voltage, and wherein said second PMOS transistor has both said a first threshold voltage implantation and said threshold voltage implantation reticle option layer;
measuring said voltage at said output pin in said second test mode when said drain and said gate are connected to said ground through a second internal a first resistance; and
comparing said voltage at said output pin in said first test mode with said voltage at said output pin in said second test mode to detect the presence of said threshold voltage implantation reticle option layer in said integrated circuit device (column 23, lines 27-30).

20. Pertaining to claim 21, Dasse teaches the method according to Claim 20 wherein said selecting of said first PMOS transistor is by a multiplex circuit and wherein said selecting of said second PMOS is by a
multiplex circuit.

21. Pertaining to claim 22, Dasse teaches the method according to Claim 20 further comprising:
amplifying said voltage at said drain and said gate of said first PMOS transistor and said second PMOS transistor to thereby generate an amplified drain and gate voltage at said output pin.

22. Pertaining to claim 23, Dasse teaches the method according to Claim 20 wherein said first PMOS transistor and said second PMOS transistor are the same size, the same layout orientation, and in close proximity.

23. Pertaining to claim 24, Dasse teaches the method according to Claim 20 wherein said first internal resistance and said second internal resistance comprise the same resistance value.

Conclusion

24. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

25. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

26. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

W. David Coleman
Primary Examiner
Art Unit 2823

WDC